Key to Midterm Exam S2
Computer Architecture

Duration: 1 hr 30 min

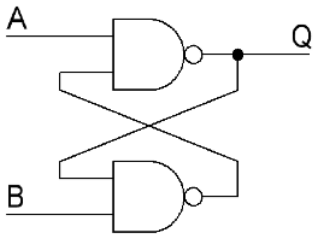
Answer on the answer sheet only.
Do not show any calculation unless you are explicitly asked.
Do not use a pencil or red ink.

Exercise 1 (9 points)

1. Convert the numbers given on the answer sheet into their **single-precision** IEEE-754 representations. Write down the final result in its **binary form** and specify the three fields.
2. Convert the **double-precision** IEEE-754 words given on the answer sheet into their associated representations. If a representation is a number, use the base-10 following form: $k \times 2^n$ where k and n are integers (either positive or negative).
3. Determine the smallest and largest absolute values of a double-precision IEEE-754 **denormalized** number. Use the following form: 2^n for the smallest number and $(1 - 2^{n1}) \times 2^{n2}$ for the largest number where n, $n1$ and $n2$ are integers (either positive or negative). Write down the base-10 numerical values of n, $n1$ and $n2$ on the answer sheet.

Exercise 2 (3 points)

Let us consider the following circuit:



1. Complete the truth table shown on the answer sheet.
2. What is the name of this circuit?

Exercise 3 (1 point)

Draw the circuit diagram of a divide-by-two circuit by using only one master-slave RS flip-flop. Answer on the answer sheet.

Exercise 4 (7 points)

Complete the timing diagrams shown on the answer sheet (up to the last vertical dotted line) for the following circuits.

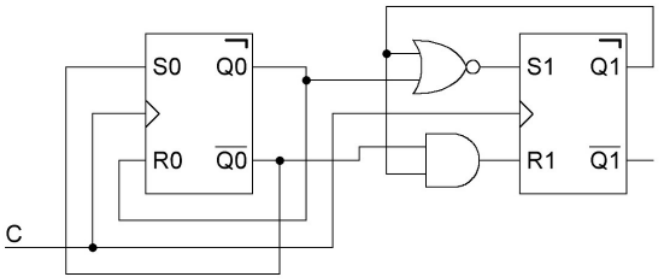


Figure 1

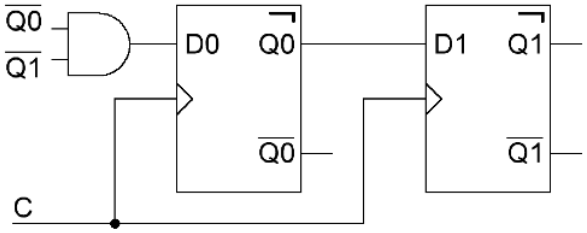


Figure 2

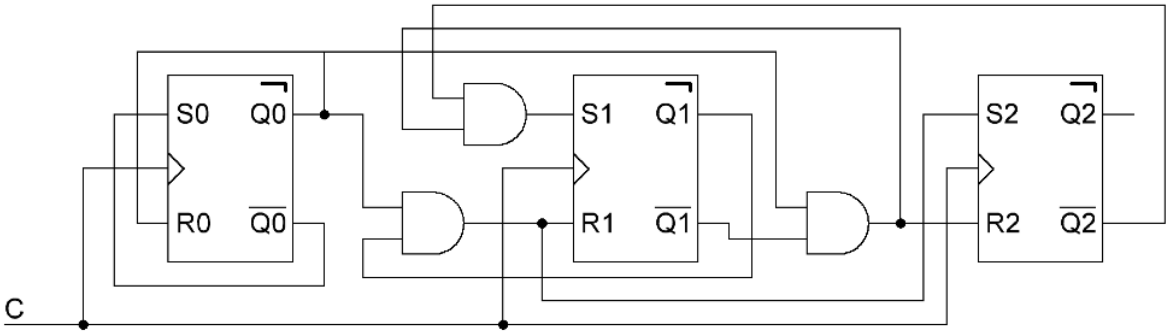


Figure 3

Last name: ..... First name: ..... Group: .....

ANSWER SHEET

Exercise 1

1.

Number	S	E	M
257	0	10000111	00000001000000000000000
78.1875	0	10000101	00111000110000000000000
0.109375	0	01111011	11000000000000000000000

2.

IEEE-754 Representation	Associated Representation
$2A48\ 0000\ 0000\ 0000_{16}$	3×2^{-348}
$FFF0\ 0000\ 0000\ 000F_{16}$	NaN
$000B\ C000\ 0000\ 0000_{16}$	47×2^{-1028}
$4000\ 0000\ 0000\ 0000_{16}$	1×2^{1}

3.

n	n1	n2
-1074	-52	-1022

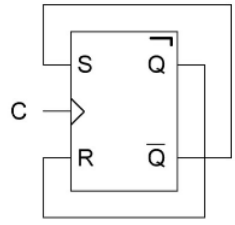
Exercise 2

A	B	Q
0	0	1
0	1	1
1	0	0
1	1	q

Name of the circuit
Active-low RS latch

Exercise 3

Divide-by-Two Circuit



Exercise 4

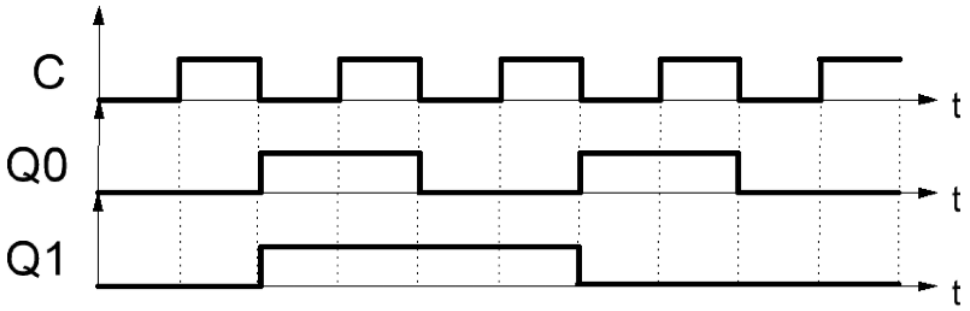


Figure 1

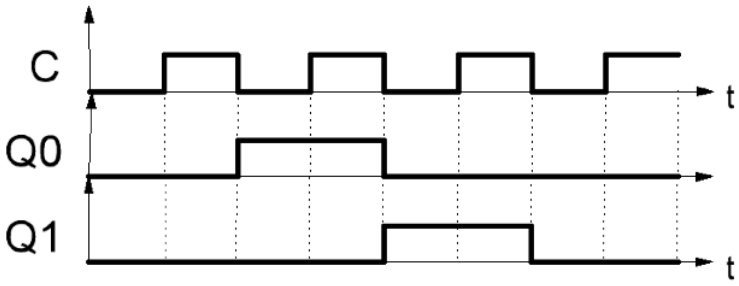


Figure 2

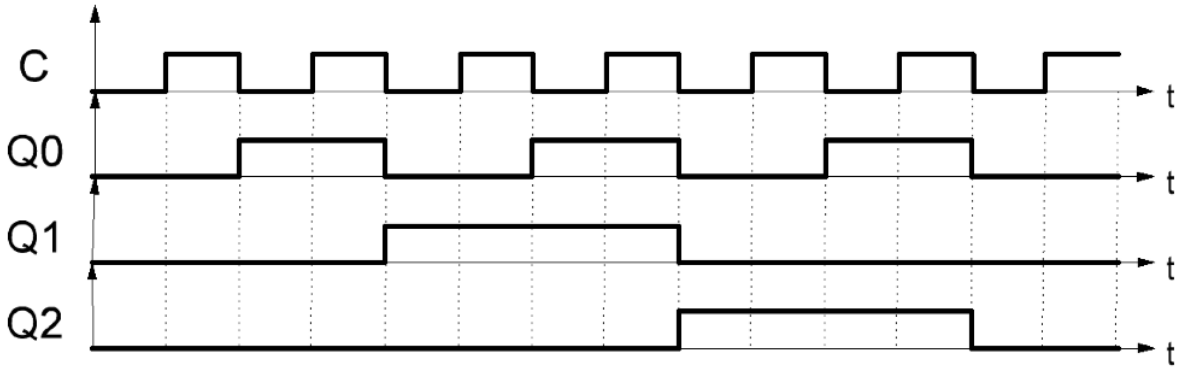


Figure 3

Feel free to use the blank space below if you need to: