

Family name: First name: Group:

ANSWER SHEET

Exercise 1

| Question | Answer |
|--|--------|
| How can we connect memory devices in order to enlarge the width? | |
| A memory has a depth of 32 Ki words. How many address lines does this memory have? | |
| A memory has a width of 16 bits and a capacity of 64 Kib. How many address lines does this memory have? | |
| A memory has a 4-bit data bus and a 15-bit address bus. In a power of two, what is the capacity in bits of this memory? | |
| An M1 memory has an 8-bit data bus and a 16-bit address bus. Two M1 memories are connected in series to build an M2 memory. What is the size of the address bus of the M2 memory? | |
| A microprocessor has a 24-bit address bus. Five address lines are used for selecting the devices. With the block address decoding, what is the maximum number of address lines that a device connected to this microprocessor can have? | |
| <p>A microprocessor has a 20-bit address bus. Using the linear address decoding, we connect this microprocessor to the following devices.</p> <ul style="list-style-type: none"> • a ROM device (15 address lines) • a RAM device (12 address lines) • a peripheral device (10 address lines) <p>How many address lines are unused in the case of the RAM device?</p> | |

Exercise 2

| Question | Answer |
|---|--------|
| What is the depth of the m memory? | |
| What is the depth of the M memory? | |
| What is the number of address lines of the m memory? | |
| What is the number of address lines of the M memory? | |
| How many memory devices should be put in parallel? | |
| How many memory devices should be put in series? | |
| How many address lines are required to control the CS input of the memory devices? | |
| When the M memory is active, how many m memory devices are active simultaneously? | |

Exercise 3

| | |
|-------------------------------|---------------------------|
| 1. ROM: RAM: P1: P2: | 2. Device-selection bits: |
|-------------------------------|---------------------------|

| | |
|---------------------------------|----------------------------|
| 3. $CS_{ROM} =$ $CS_{RAM} =$ | $CS_{P1} =$ $CS_{P2} =$ |
|---------------------------------|----------------------------|

4.

| Device | Lowest Address | Highest Address |
|--------|----------------|-----------------|
| ROM | | |
| RAM | | |
| P1 | | |
| P2 | | |

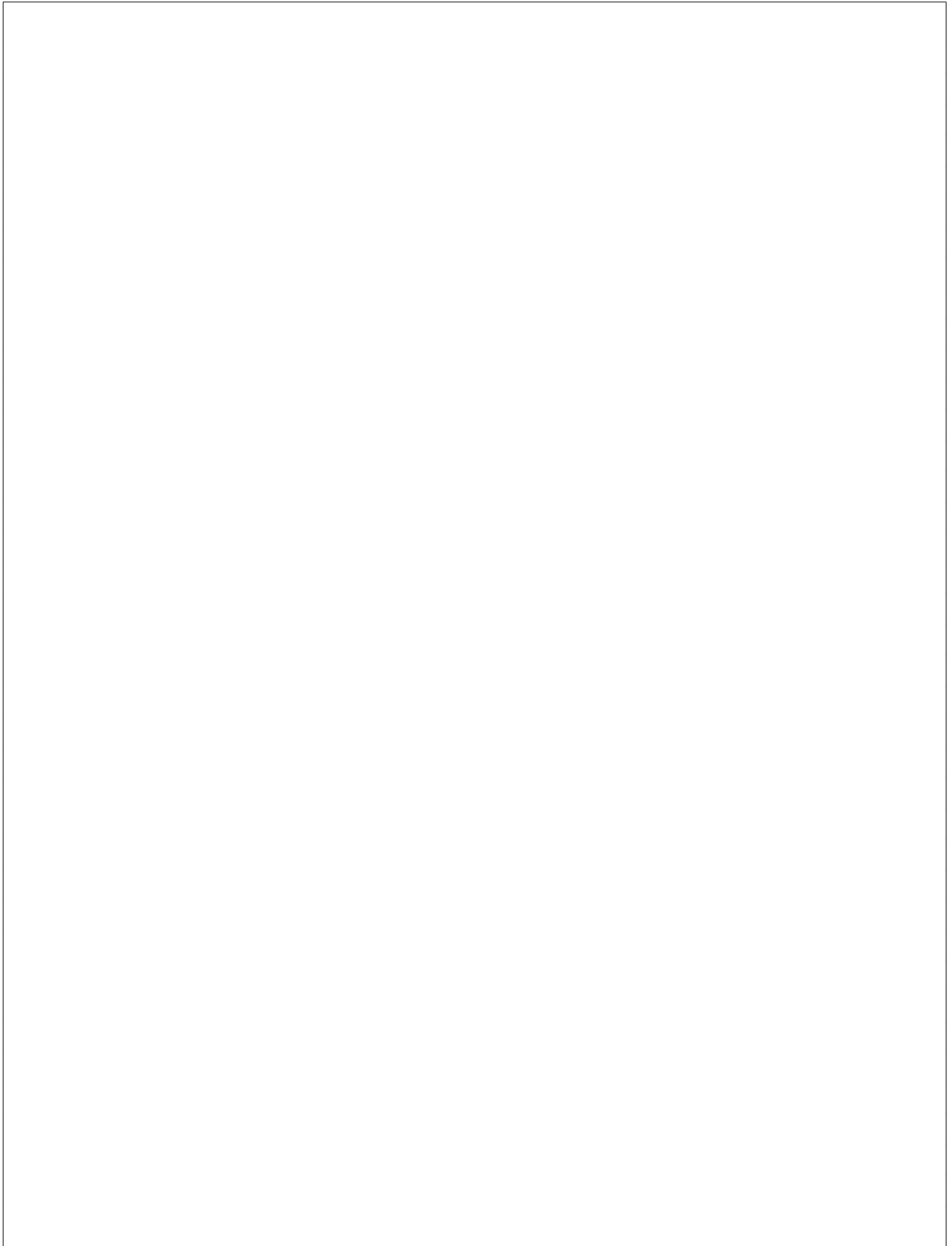
Exercise 4

| | |
|---|---|
| 1. ROM : RAM : P1 : P2 : | 2. Can we use the linear address decoding? (Yes or No) <hr/> 3. Device-selection bits: |
|---|---|

| | |
|-------------------------------------|--------------------------------|
| 4. $CS_{ROM} =$ $CS_{RAM} =$ | $CS_{P1} =$ $CS_{P2} =$ |
|-------------------------------------|--------------------------------|

| Device | 5. | | 6. |
|--------|----------------|-----------------|------------------|
| | Lowest Address | Highest Address | Number of Images |
| ROM | | | |
| RAM | | | |
| P1 | | | |
| P2 | | | |

Feel free to use the blank space below if you need to:

A large, empty rectangular box with a thin black border, occupying most of the page. It is intended for the student to use for writing or drawing if needed.