Final Exam S2
Computer Architecture

Duration: 1 hr 30 min

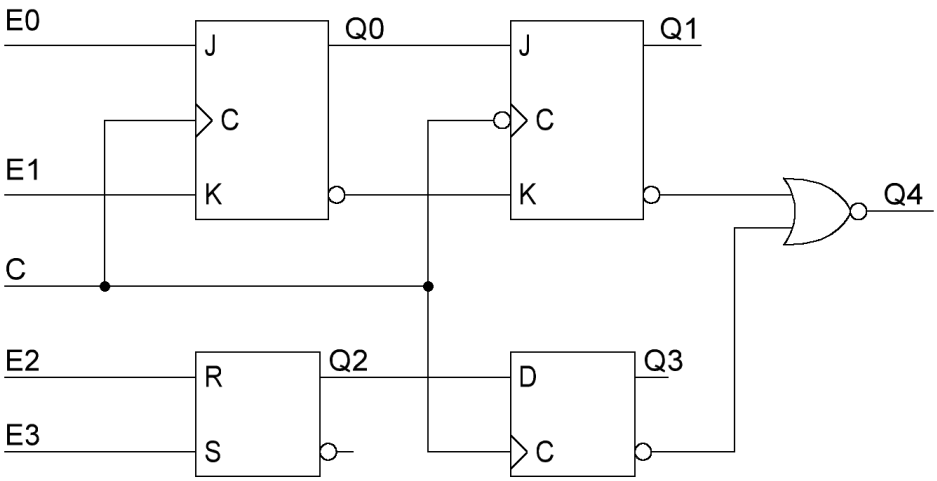
Answer on the answer sheet only.
Do not show any calculation unless you are explicitly asked.
Do not use red ink.

Exercise 1 (5 points)

1. Convert the numbers given on the answer sheet into their **single-precision** IEEE-754 representations. Write down the final result in its **binary form** and specify the three fields.
2. Convert the **double-precision** IEEE-754 words given on the answer sheet into their associated representations. If a representation is a number, use the base-10 following form: $k \times 2^n$ where k and n are integers (either positive or negative).

Exercise 2 (5 points)

Complete the timing diagrams shown on the answer sheet (up to the last vertical dotted line) for the circuit below.



Exercise 3 (6 points)

The table shown on the answer sheet gives the sequence of a counter we want to design. This counter should be made up of JK flip-flops.

1. Complete the table shown on the answer sheet.
2. Write down the most simplified expressions of *J* and *K* for each flip-flop on the answer sheet. **Complete the Karnaugh maps for the solutions that are not obvious**. An obvious solution does not have any logical operations apart from the complement (for instance: J0 = 1, K1 = $\overline{Q2}$).

Exercise 4 (4 points)

We want to build a 2-MiB ROM device (labelled ***M***) from several 16-KiB ROM devices (labelled ***m***). The ***M*** device has a 16-bit data bus. The ***m*** devices have an 8-bit data bus. Answer the questions on the answer sheet.

Last name: ..... First name: ..... Group: .....

ANSWER SHEET

Exercise 1

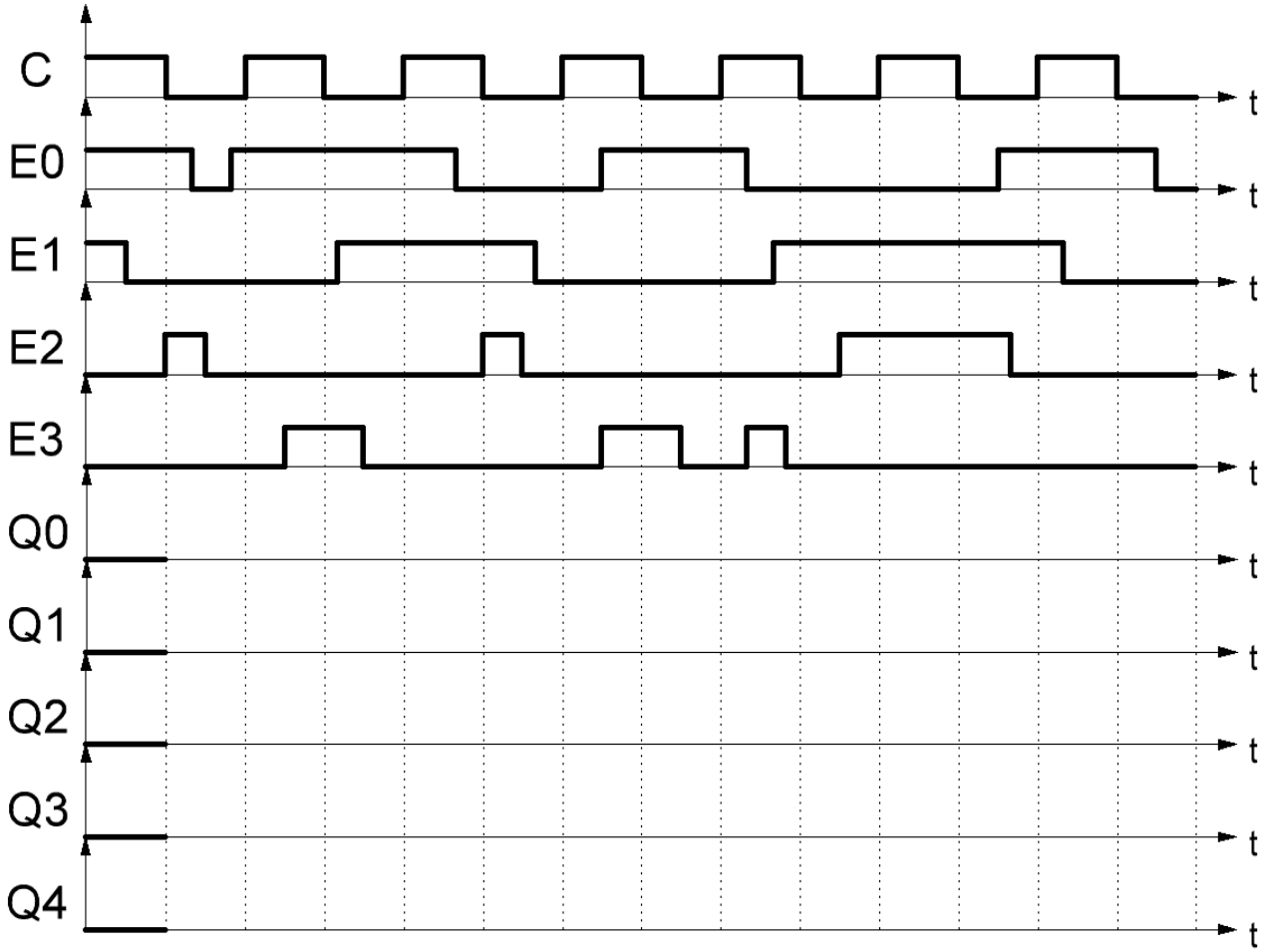
1.

Number	S	E	M
-146.3125			
0.34375			

2.

IEEE-754 Representation	Associated Representation
2468000000000000_{16}	
$7FFF000000000000_{16}$	
0006800000000000_{16}	

Exercise 2



Exercise 3

Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
1	1	1						
1	0	0						
1	0	1						
1	1	0						
0	1	1						
0	0	1						
0	0	0						

Do not use Karnaugh maps for obvious solutions.

Q1 Q0

J0	00	01	11	10
Q2 0				
Q2 1				

J0 =

Q1 Q0

K0	00	01	11	10
Q2 0				
Q2 1				

K0 =

Q1 Q0

J1	00	01	11	10
Q2 0				
Q2 1				

J1 =

Q1 Q0

K1	00	01	11	10
Q2 0				
Q2 1				

K1 =

Q1 Q0

J2	00	01	11	10
Q2 0				
Q2 1				

J2 =

Q1 Q0

K2	00	01	11	10
Q2 0				
Q2 1				

K2 =

Exercise 4

Question	**Answer**
What is the depth of the ***m*** memory?	
What is the depth of the ***M*** memory?	
What is the number of address lines of the ***m*** memory?	
What is the number of address lines of the ***M*** memory?	
How many memory devices should be put in parallel?	
How many memory devices should be put in series?	
How many address lines are required to control the *CS* input of the memory devices?	
When the ***M*** memory is active, how many ***m*** memory devices are active simultaneously?	

Feel free to use the blank space below if you need to: