Key to Final Exam S2
Computer Architecture

Duration: 1 hr 30 min

Answer on the answer sheet only.
Do not show any calculation unless you are explicitly asked.
Do not use red ink.

Exercise 1 (5 points)

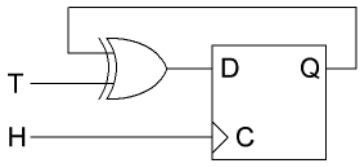
1. Convert the numbers given on the answer sheet into their **single-precision** IEEE-754 representations. Write down the final result in its **binary form** and specify the three fields.
2. Convert the **double-precision** IEEE-754 words given on the answer sheet into their associated representations. If a representation is a number, use the base-10 following form: $k \times 2^n$ where k and n are integers (either positive or negative).

Exercise 2 (5 points)

Answer the questions on the answer sheet.

Exercise 3 (5 points)

1. Wire the flip-flops (figure 1) in order to design a **modulo-14 asynchronous up counter**.
2. Wire the flip-flops (figure 2) in order to design a **modulo-14 asynchronous down counter**.
3. Complete the timing diagrams shown on the answer sheet (up to the last vertical dotted line) for the following circuit.



Exercise 4 (6 points)

The table shown on the answer sheet gives the sequence of a counter we want to design. This counter should be made up of JK flip-flops.

1. Complete the table shown on the answer sheet.
2. Write down the most simplified expressions of J and K for each flip-flop on the answer sheet. **Complete the Karnaugh maps for the solutions that are not obvious**. An obvious solution does not have any logical operations apart from the complement (for instance: J0 = 1, K1 = $\overline{Q2}$).

Last name: ..... First name: ..... Group: .....

ANSWER SHEET

Exercise 1

1.

Number	S	E	M
217.25	0	10000110	10110010100000000000000
0.21875	0	01111100	11000000000000000000000

2.

IEEE-754 Representation	Associated Representation
$423E\ 0000\ 0000\ 0000_{16}$	15×2^{33}
$8003\ 8000\ 0000\ 0000_{16}$	-7×2^{-1027}
$7FF0\ 0000\ 0000\ 0000_{16}$	$+\infty$

Exercise 2

Question	Answer
A memory has a depth of 64 Ki words. How many address lines does this memory have?	16 lines
A memory has an 8-bit data bus and a 16-bit address bus. In a power of two, what is the capacity in bits of this memory?	2^{19} bits
An **M1** memory has a 16-bit data bus and a 32-bit address bus. Two **M1** memories are connected in series to build an **M2** memory. What is the size of the address bus of the **M2** memory?	33 bits
A microprocessor has a 20-bit address bus. Three address lines are used for selecting the devices. With the linear address decoding, what is the maximum number of address lines that a device connected to this microprocessor can have?	17 lines
A microprocessor has a 24-bit address bus. Using the linear address decoding, we connect this microprocessor to the following devices. • a ROM device (20 address lines) • a RAM device (15 address lines) • a peripheral device (10 address lines) How many bits are unused in the case of the RAM device?	6 bits

Exercise 3

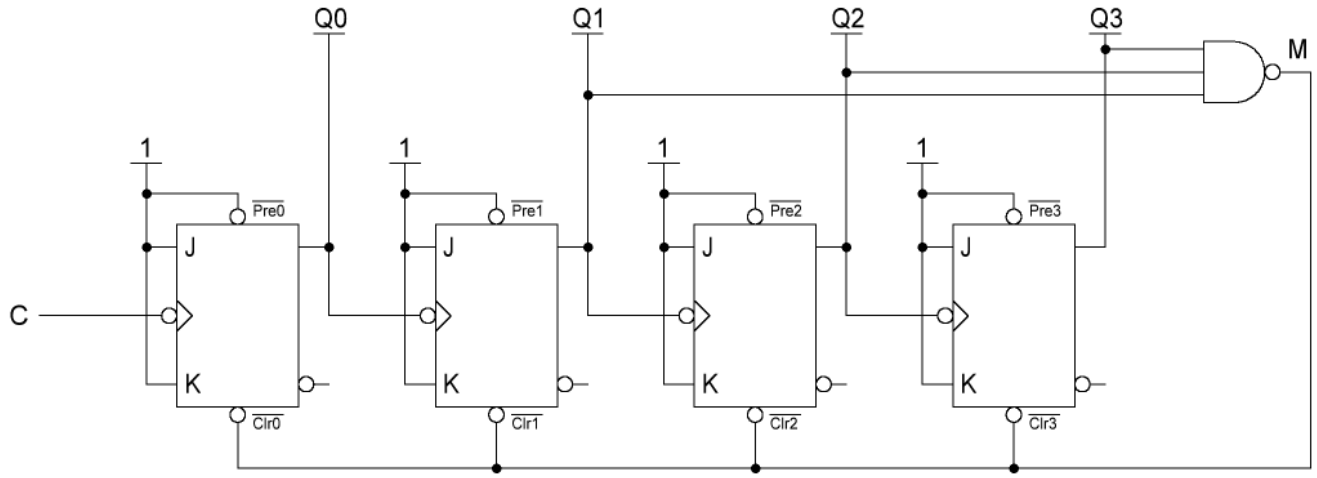


Figure 1

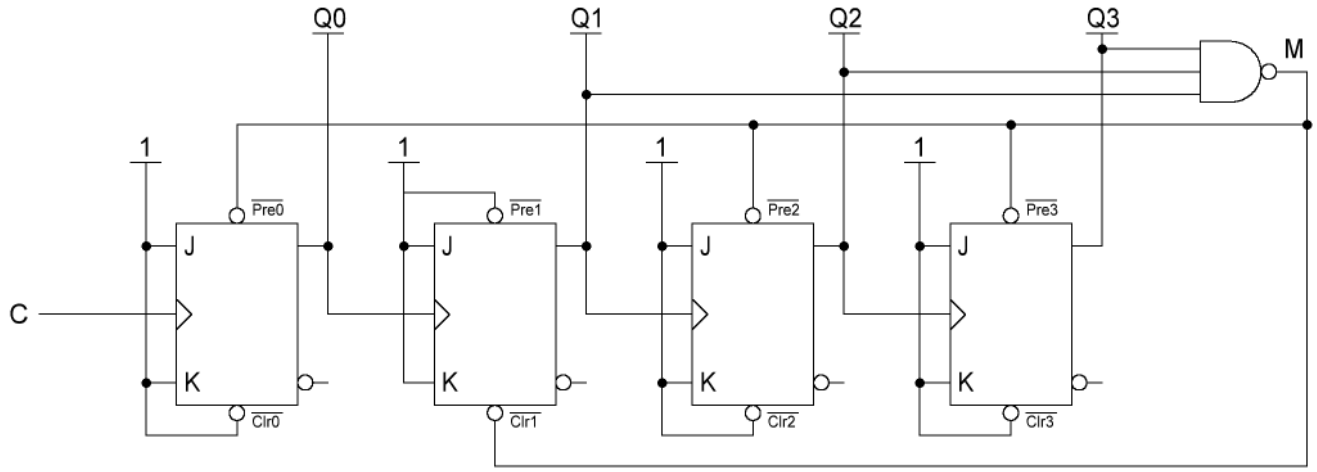
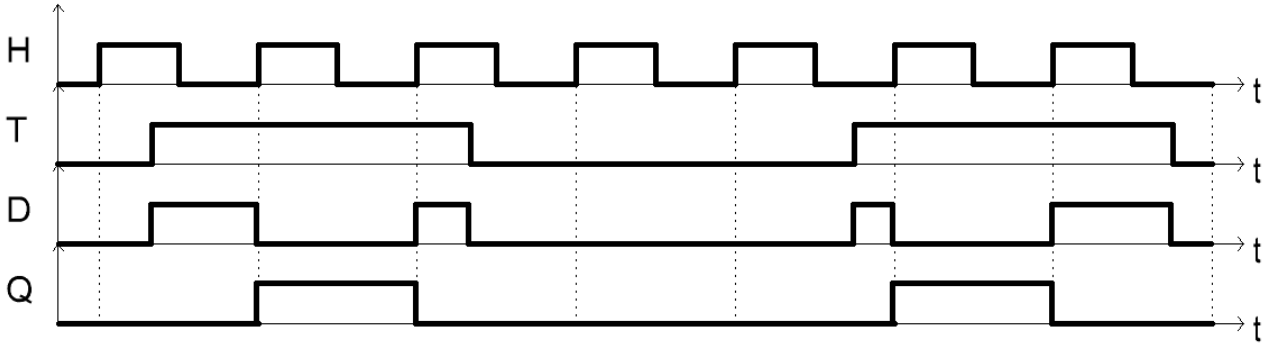


Figure 2



Exercise 4

Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
1	1	1	Φ	0	Φ	1	Φ	1
1	0	0	Φ	0	0	Φ	1	Φ
1	0	1	Φ	0	1	Φ	Φ	1
1	1	0	Φ	1	Φ	0	0	Φ
0	1	0	0	Φ	Φ	1	1	Φ
0	0	1	0	Φ	0	Φ	Φ	1
0	0	0	1	Φ	1	Φ	1	Φ

Do not use Karnaugh maps for obvious solutions.

J0 (Q2 \ Q1 Q0)	00	01	11	10
0	1	Φ	Φ	1
1	1	Φ	Φ	0

J0 = $\overline{Q2}$ + $\overline{Q1}$

K0 (Q2 \ Q1 Q0)	00	01	11	10
0				
1				

K0 = 1

J1 (Q2 \ Q1 Q0)	00	01	11	10
0	1	0	Φ	Φ
1	0	1	Φ	Φ

J1 = $\overline{Q2}$. $\overline{Q0}$ + Q2.Q0 = $\overline{Q2 \oplus Q0}$

K1 (Q2 \ Q1 Q0)	00	01	11	10
0	Φ	Φ	Φ	1
1	Φ	Φ	1	0

K1 = $\overline{Q2}$ + Q0

J2 (Q2 \ Q1 Q0)	00	01	11	10
0	1	0	Φ	0
1	Φ	Φ	Φ	Φ

J2 = $\overline{Q1}$.$\overline{Q0}$

K2 (Q2 \ Q1 Q0)	00	01	11	10
0	Φ	Φ	Φ	Φ
1	0	0	0	1

K2 = Q1.$\overline{Q0}$

Feel free to use the blank space below if you need to: